23. The improvement of claim 22 including a data processing capability responsive to data through said separate path delivered to said output port.

24. The improvement of claim 23 wherein said separate address information path is from an address register in said memory assembly through a serializer to an output buffer in said memory assembly, and said processing instruction is from a timing register through a serializer to said output buffer in said memory assembly.

25. The improvement of claim 22 wherein said processing instruction disables entry of to be stored information into said plurality of addressable storage locations.

26. The improvement of claim22 wherein said processing instruction employs an unused in a standard storage event condition on a terminal in combination with a burst stop command in said memory assembly.

27. In an addressable random access memory of the type having a plurality of storage locations, being responsive in processing to data increments having an address portion and a to be stored portion, and having a register for direction of specific data increments to specific ones of said plurality of storage locations, the method of verifying that the location in said plurality of storage locations to which a specific increment of said data increments was directed is the location in which it resides,

comprising the steps of:

directing said address information portion of said data, appearing in a data path to said plurality of addressable storage locations, through a separate path around said plurality of addressable storage locations, to an output location,

providing at said output location access in said register to the assigned location in which each data increment was to be stored, and,

comparing the data in said separate path with said register for a difference of storage location.

28. The method of claim 27 wherein said separate path is a path between an address register element and said output buffer element.

29. The method of claim 28 wherein said register for direction of specific data increments to specific ones of said plurality of storage locations is a mode register element, and said output location is an output buffer element.

30. The method of claim 29 wherein a copy of the entries in said mode register element is stored in separate computation apparatus connected to said output buffer element.

31. In an addressable random access memory of the type having a plurality of storage locations, being responsive in processing to data increments having an address portion and a to be stored portion, and having a register for direction of specific data increments to specific ones of said plurality of storage locations, the method of tuning the timing of said random access memory assembly for optimization of said address portion of a data increment and the clock function of said memory,

comprising the steps of:

directing said address information portion of said data, appearing in a data path to said plurality of addressable storage locations, through a separate path around said plurality of addressable storage locations, to an output location,

providing at said output location separately stored increments said clock function and separately stored address portions of said data, and,

comparing the data in said separately stored address portions of said data with a corresponding pulse from said clock function and identifying events where said clock function pulse occurred other than during said address portion of said data.path with said register for a difference of storage location.

32. The method of claim 31 including the step of adjusting the output of said clock function to position said corresponding pulse to the center of the duration of said address portion of said data.

33. In an addressable random access memory having a plurality of data array banks arranged in columns and rows, having provision for read and write signals in separate cycles to said banks multiplexed into a common data bus and having power driving elements for each of said banks,
the improvement for adjustment of timing skew in operation of said memory comprising:
means for placing into said common data bus, in one said read cycle, during the duration of a column access time, a uniform set of serial signals, and,
means for holding enablement of delivery of said uniform set of serial signals until the start of access of a column.

34. The improvement of claim 33 including an align signal operable to disconnect data array banks from said common data bus.

35. In an addressable random access memory assembly,
said assembly having an input port and an output port,
said assembly having a plurality of drivers, driving, through a common communication channel data path, data array banks arranged in columns and rows,
the improvement comprising:
means providing separate read and write cycles, and,
means ,taking place during a said read cycle, for redirection of address data, from a said data path to said data array banks, to a data path to at least said output port.

36.The improvement of claim 35 wherein during said read cycle said address data is received through

2 a column decoder.

1 37. The improvement of claim 36 wherein during said read cycle said address data is held until the
2 beginning of the address.

The added processing fees are calculated as follows.

At filing 20 total claims were paid for of which 5 were independent resulting in 2 excess independent claims being paid for at that time.

In this preliminary amendment 17 total additional claims are added of which 5 are additional independent claims resulting in a total of 37 total claims of which 17 are excess over 20 at $18 each = $306 together with 5 excess independent claims at $84 each =$420 for a total of $ 726. A deposit account authorization is provided herewith.

Enclosed is a supplemental Information Disclosure with copies of references encountered in prosecution in the parent application Ser.No. 09/419,514 filed 10/18/99.

Respectfully submitted,
Alvin J. Riddles 10/16/02
Alvin J. Riddles
Reg. No. 17862
(914) 472 - 0644 (203) 746 - 3470

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